REMARKS

Claims 1 through 11 are pending in this Application, of which claims 2 through 4 have been allowed. Claims 1, 5, 10 and 11 have been amended. Care has been exercised to avoid the introduction of new matter. Indeed, adequate descriptive support for the present Amendment should be apparent throughout the originally filed disclosure as, for example, Fig. 23 and the related discussion thereof in the written description of the specification, noting page 16, lines 25 through 28. Applicants would further note that claim 5 has been amended by incorporating the limitations of claim 8 therein, and claim 8 deleted. Claims 10 and 11 have also been placed in independent form. Applicants submit that the present Amendment does not generate any new matter issue.

Claims 5 and 6 were rejected under the second paragraph of 35 U.S.C. § 112.

In the statement of the rejection the Examiner asserted that the expression "another element" in claims 5 and 6 render the claims indefinite. This rejection is traversed.

Firstly, the Examiner should be aware that indefiniteness under the second paragraph of 35 U.S.C. § 112 is a **question of law**. *Personalized Media Communications LLC v. U.S. International Trade Commission, 161 F.3d 696, 48 USPQ2d 1880 (Fed. Cir. 1998)*; *Tillotson, Ltd v. Wlaboro Corp., 831 F.2d 1033, 4 USPQ2d 1450 (Fed. Cir. 1987)*; *Orthokinetics Inc. v. Safety Travel Chairs Inc., 806 F.2d 1565, 1 USPQ2d 1081 (Fed. Cir. 1986)*. Accordingly, in rejecting a claim under the second paragraph of 35 U.S.C. § 112, the Examiner must provide a basis in fact and/or cogent technical reasoning to support the ultimate legal conclusion that one having ordinary skill in the art, with the supporting specification in hand, would not be able to reasonably ascertain the scope of protection defined by a claim. *In re Okuzawa, 537 F.2d 545,*

190 USPQ 464 (CCPA 1976). Significantly, consistent judicial precedents holds that **reasonable precision** in light of the particular subject matter involved is all that is required by the second paragraph of 35 U.S.C. § 112. *Zoltek Corp. v. United States, 48 Fed. Cl. 240, 57 USPQ2d 1257 (Fed. Cl. 2000)*; *Miles Laboratories, Inc. v. Shandon, Inc., 997 F.2d 870, 27 USPQ2d 1123 (Fed. Cir. 1993)*; *North American Vaccine, Inc. v. American Cyanamid Co., 7 F.3d 1571, 28 USPAP2d 1333 (Fed. Cir. 1993)*; *U.S. v. Telectronics Inc., 857 F.2d 778, 8 USPQ2d 1217 (Fed. Cir. 1988)*; *Hybritech, Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 231 USPQ (Fed. Cir. 1986).* Applicants stress that claims must be interpreted as one having ordinary skill in the art would have interpreted the claims in light of and consistent with the supporting specification. *Zoltek Corp. v. United States, supra*; *Miles Laboratories, Inc. v. Shandon, Inc., supra.*

In applying the above legal tenets to the exigencies of the case, Applicants submit that the Examiner did not discharge the initial burden of establishing a *prima facie* basis to deny patentability to the claimed invention under the second paragraph of 35 U.S.C. § 112. The Examiner did not even begin to attempt to establish a *prima facie* case under the second paragraph of 35 U.S.C. § 112. The Examiner just announced the conclusion that the claimed invention was indefinite and queried: "What is another element?" The Examiner's approach presumes not only that one having ordinary skill in the art is devoid of any skill but also that one having ordinary skill in the art did not read the supporting specification. The Examiner's approach is, therefore, legally erroneous.

The Examiner should also be aware that only claims "not amenable to construction" or "insolubly ambiguous" are indefinite. *See Novo Indus., L.P. v. Micro Molds Corp., 350 F.d3 1348, 1353 [69 USPQ2d 1128] (Fed. Cir. 2003)*; *Honeywell Int'l, 341 F.3d at 1338; Exxon Research & Eng'g Co. v. United States, 265 F.3d 1371, 1375 [60 USPQ2d 1272] (Fed. Cir.*

2002). Thus, the definiteness of claim terms depends on whether those terms can be given any reasonable meaning.

Applicants submit that one having ordinary skill in the art would have understood that an interconnection structure forms a circuit by connecting different elements in the device, which circuit is accessible outside of the device. A dummy component does not function within any such circuit and, hence, does not electrically connect one functional element to another, as one having ordinary skill in the art would have understood. Thus, one having ordinary skill in the art would have understood the meaning of "another element" as an element other than the first conductive layer that is functional in the semiconductor device so that the device can satisfactorily perform.

Lest there by any doubt, Applicants submit herewith as Exhibit A a copy of pages 527 and 528 from a basic textbook on semiconductor processing by Badih El-Kareh entitled "FUNDAMENTALS OF SEMICONDUCTOR PROCESSING TECHNOLOGIES", copyright 1995. Based upon Exhibit A, it should be apparent that one having ordinary skill in the art would have understood the fundamental concept that interconnect structures connect basic elements of the semiconductor device to form a circuit. Accordingly, one having ordinary skill in the art would have no difficulty understanding the scope of claims 5 and 6, particularly when reasonably interpreted in light of and consistent with the written description of the specification, which is the judicial standard. *Miles Laboratories, Inc. v. Shandon, Inc., supra.*

Applicants, therefore, submit that the imposed rejection of claims 5 and 6 under the second paragraph of 35 U.S.C. § 112 is not legally viable and, hence, solicit withdrawal thereof.

Claim 11 was rejected under the first paragraph of 35 U.S.C. § 112 for lack of adequate enabling support.

In the statement of the rejection the Examiner asserted it is unclear how the dummy hole was formed to reach the second interconnection portion with the small line width. This rejection is traversed.

Claim 11 has been amended to address the issue raised by the Examiner. Clearly, one having ordinary skill in the art would have understood how the dummy hole was formed to reach the second interconnection with the small line with, noting Fig. 22 and the related discussion thereof in the written description of the specification. Under such circumstances, there is no basis upon which to question enablement. Indeed, enablement must be presumed absent any cogent technological reason to maintain otherwise. *In re Brana, 51 F.3d 1560, 34 USPQ2d 1436 (Fed. Cir. 1995)*; *In re Marzocchi, 439 F.2d 220, 169 USPQ 367 (CCPA 1971).*

Based upon the foregoing, Applicants submit that the imposed rejection of claim 11 under the first paragraph of 35 U.S.C. § 112 for lack of adequate enabling support is not legally viable and, hence, solicit withdrawal thereof.

Claim 1 was rejected under 35 U.S.C. § 102 for lack of novelty as evidenced by Saito et al.

In the statement of the rejection the Examiner referred to Fig. 18 of Saito et al., and pointed to elements asserted to correspond to those of the claimed invention. This rejection is traversed.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically

claimed invention is placed into the recognized possession of one having ordinary skill in the art. *Dayco Prods., Inc. v. Total Containment, Inc., 329 F.3d 1358, 66 USPQ2d 1801 (Fed. Cir. 2003)*; *Crown Operations International Ltd. v. Solutia Inc., 289 F.3d 1367, 62 USPQ2d 1917 (Fed. Cir. 2002)*. There is a fundamental difference between the claimed interconnect structure and the structure disclosed by Saito et al. that scotches the factual determination that Saito et al. disclose an interconnection structure identically corresponding to that claimed.

Specifically, claim 1 has been clarified by reciting that the insulating layer is a single insulating layer, thereby completely distinguishing over the structure disclosed by Saito et al. This is because the Fig. 18 structure of Saito et al. relied upon by the Examiner contains a groove that is **not**, repeat **not**, formed within the same insulating layer as the hole. In this respect Applicants would point out that there are **four**, repeat **four**, insulating layers in which the groove and hole are formed, i.e., 24b, 24c, 26b and 26c.

The above argued structural difference between the claimed interconnection structure and the structure disclosed by Saito et al. undermines the factual determination that Saito et al. disclose a structure identically corresponding to that claimed. *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc., 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992)*; *Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986)*. Applicants, therefore, submit that the imposed rejection of claim 1 under 35 U.S.C. § 102 for lack of novelty as evidenced by Saito et al. is not factually viable and, hence, solicit withdrawal thereof.

Claims 5 through 11 were rejected under 35 U.S.C. § 103 for obviousness predicated upon Wang.

In the statement of the rejection the Examiner asserted that certain elements of the structure disclosed by Wang et al. correspond to elements of the claimed invention, and then attributed any difference to design choice. This rejection is traversed as factually and legally erroneous.

Initially, claim 5 has been clarified by incorporating limitations of claim 8 therein and canceling claim 8. Thus, claim 5 requires, *inter alia*, a second conductive layer with first and second interconnection portions having a large line within a small line width. The Examiner should be aware that when imposing a rejection under 35 U.S.C. § 103 the Examiner is required to specifically identify a source in the applied prior art for each claim limitation as well as a factual basis to support the asserted motivation. *Smiths Industries Medical System v. Vital Signs Inc., 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999).* That burden has not been discharged.

Further, Applicants take issue with the Examiner's rubric "obvious design choices", because such an approach has been repeatedly judicially condemned as legally erroneous. See, for example, *In re Chu, 66 F.3d 292, 36 USPQ2d 1089 (Fed. Cir. 1995)*; *In re Gal, 980 F.2d 717, 25 USPQ2d 1076 (Fed. Cir. 1992)*; *In re Bezombes, 420 F.2d 1070, 164 USPQ 387 (CCPA 1970).* In this respect, Applicants would stress that regardless of the source of motivation, the Examiner is still required to provide **facts**. *Teleflex Inc. v. Ficosa North America Corp., 299 F.3d 1313, 63 USPQ2d 1374 (Fed. Cir. 2002).*

Based upon the foregoing it should be apparent that the *prima facie* basis to deny patentability to the claimed invention has not been established for lack of the requisite factual basis and want of the requisite realistic motivation. Applicants, therefore, submit that the

imposed rejection of claims 5 through 11 under 35 U.S.C. § 103 for obviousness predicated upon Wang is not factually or legally viable and, hence, solicit withdrawal thereof.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Arthur J. Steiner
Registration No. 26,106

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 AJS:bjs:ntb
Facsimile: 202.756.8087
Date: October 26, 2005

Please recognize our Customer No. 20277 as our correspondence address.

EXHIBIT A

FUNDAMENTALS of SEMICONDUCTOR PROCESSING TECHNOLOGIES

by

Badih El-Kareh

IBM Corporation

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Chapter 8

Contact and Interconnect Technology

With J. G. Ryan, IBM

8.0 Introduction

The preceding chapters described how to define p- and n-type doped regions in single crystal and polycrystalline material. Those regions are the basic elements of semiconductor devices that must be connected in a specific configuration to form the desired circuit. The circuit must also be accessible to the "outside world" through conducting pads for testing with metal probes and for bonding to metal pins to complete the packaged chip. While doped silicon and polysilicon conduct electricity, they are of limited use for interconnections, mainly because of their prohibitively large resistance and lack of interconnecting flexibility. Therefore, at least one low-resistance conductor film must be deposited and patterned to contact and interconnect the different regions on the chip. Several single- and multi-metal systems are available for this purpose. Because of its high conductivity, compatibility with a silicon-base technology, and low processing cost, aluminum is the most widely used interconnect material.

One simple metallization process sequence consists of covering the wafer with an insulator, patterning and etching contact openings in the insulator, and then depositing and defining an aluminum film to form both the contacts and interconnecting leads (Fig. 8.1). Aluminum, however, penetrates silicon to a certain depth that depends primarily on the metal composition and thermal cycle following metal deposition. As the minimum feature size is reduced and the device dimensions shrink, so does the junction depth, increasing the probability for the penetrating aluminum to reach the junction and cause excessive leakage. To avoid metal penetration, it is necessary to modify the contact metallurgy by, e.g., adding silicon to the metal, as discussed below.

Another concern with reducing the depth of the junction is the inevitable increase in its sheet and contact resistances. Metal silicides are frequently used to reduce these resistances. Barrier metals are deposited on silicides to protect the films and interfaces with silicon from diffusing species during subsequent processing.

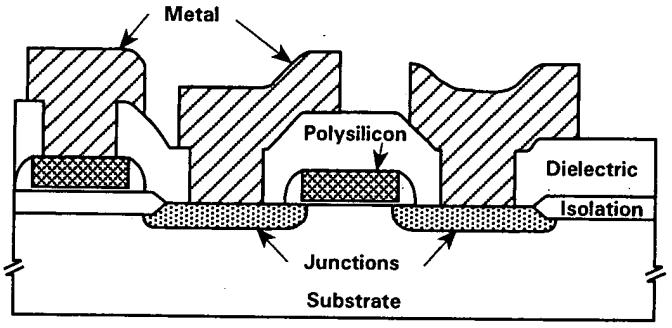

Fig. 8.1 Simplified metallization process illustrating the definition of contacts and interconnections.

Reducing the minimum feature size is typically coupled with decreasing the depth of focus of the lithographic tools (Chap. 4). This sets a limit on the allowable wafer topography, requiring techniques to planarize (level) the wafer surface prior to contact and metal definition. Also, a concomitant increase in the achievable number of circuits per unit area necessitates the use of multilevel metallization (MLM) systems to increase the interconnecting flexibility, particularly in logic designs (Fig. 8.2).

The definition and performance of metallization systems are now dominant factors in determining circuit density and speed. Key features of a metallization system are the contacting scheme, the interlevel dielectrics, the interconnecting metals, and the reliability of the metallization system. The first part of this chapter deals with contact metallurgies and discusses the different materials and techniques used to form barriers and silicides. The second part describes materials used to insulate conductors and techniques to deposit and planarize the dielectrics. The deposition, definition and reliability of interconnecting metals are discussed in the third part.

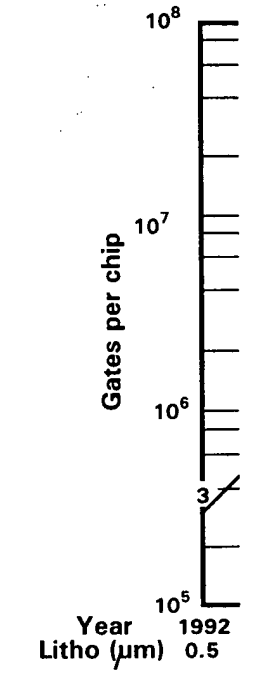

Fig. 8.2 Proj
function of n

8.1 Contact Metallu

When contact is mac
potential (barrier) ty
materials. Contacts
categorized as non-
barrier type diodes).
"transparent" to cu
voltage characteristic
displayed across the
conductor surface
Ohmic contacts are
R_c (in Ohm-cm²) th
interface between
above $\simeq 10^{19}\ cm^{-3}$, R
concentrations great
sub-micron contacts
fying contact allows